ABSTRACT OF THE DISCLOSURE

An increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data. In one embodiment, the increment/decrement circuit includes a delay circuit block operable to receive and align the debug data. First and second mask circuits are connected in parallel to the delay circuit block in order to select and assert portions of the aligned debug data for incrementing and decrementing, respectively. An accumulation circuit is connected to the first mask circuit and the second mask circuit for generating an accumulated value based on the outputs of the mask circuits.